AD-A146 184 HEATSINK REQUIREMENTS FOR COHERENT OPERATION OF HIGH-POWER SEMICONDUCTOR.. (U) AEROSPACE CORP EL SEGUNDO CA ELECTRONICS RESEARCH LAB E M GARMIRE ET AL. 1/1

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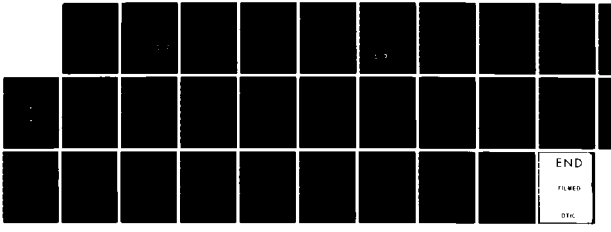

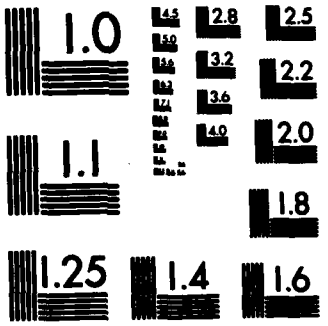

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REPORT SD-TR-84-28

(12)

Heatsink Requirements for Coherent Operation of High-Power Semiconductor Laser Arrays

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27 August 1984

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This report was submitted by The Aerospace Corporation, El Segundo, CA 90245, under Contract No. F04701-83-C-0084 with the Space Division, P.O. Box 92960, Worldway Postal Center, Los Angeles, CA 90009. It was reviewed and approved for The Aerospace Corporation by D. H. Phillips, Director, Electronics Research Laboratory. Lt Charles C. Neidhart, SD/YKXL, was the project officer for the Mission-Oriented Investigation and Experimentation (MOIE) Program.

This report has been reviewed by the Public Affairs Office (PAS) and is releasable to the National Technical Information Service (NTIS). At NTIS, it will be available to the general public, including foreign nationals.

This technical report has been reviewed and is approved for publication. Publication of this report does not constitute Air Force approval of the report's findings or conclusions. It is published only for the exchange and stimulation of ideas.

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Office, AF Space Technology Center

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REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER SD-TR-84-28	2. GOVT ACCESSION NO. AD-A146184	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) HEATSINK REQUIREMENTS FOR COHERENT OPERATION OF HIGH-POWER SEMICONDUCTOR LASER ARRAYS		5. TYPE OF REPORT & PERIOD COVERED 6. PERFORMING ORG. REPORT NUMBER TR-0084(4925-04)-3
7. AUTHOR(s) E. M. Garmire and Michael T. Tavis		8. CONTRACT OR GRANT NUMBER(s) F04701-83-C-0084
9. PERFORMING ORGANIZATION NAME AND ADDRESS The Aerospace Corporation El Segundo, Calif. 90245		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
11. CONTROLLING OFFICE NAME AND ADDRESS Space Division Los Angeles Air Force Station Los Angeles, Calif. 90009		12. REPORT DATE 27 August 1984 13. NUMBER OF PAGES 37
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office)		15. SECURITY CLASS. (of this report) Unclassified 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)
Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

AlGaAs arrays	Heatsinks	PATRAN
Broad-area laser	Laser-diode arrays	Shaped heatsinks
Diamond Heatsinks	NASTRAN	Thermal analysis
Diffraction synchronization		

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The heatsink requirements for coherent operation of laser-diode arrays are examined through thermal analysis of semi-infinite heatsinks and the phase locking of laser diodes. The thermal analysis is extended to shaped heatsinks by the use of PATRAN and NASTRAN computer programs. It is shown that mounting laser-diode arrays at the edge of semi-infinite copper heatsinks results in temperature variations between individual laser-diode elements that are too large to permit coherent operation except at

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19. KEY WORDS (Continued)

20. ABSTRACT (Continued)

relatively low power levels. It is also shown that the use of diamond and shaped heatsinks makes it possible to operate large arrays coherently to high optical output levels.

PREFACE

The authors are indebted to Bill Layton for providing extensive assistance in the use of the PATRAN and NASTRAN computer programs.

CONTENTS

FIGURES

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I. INTRODUCTION

The GaAs (gallium arsenide) laser array, in a quasibroad-area geometry, was first reported by Scifres, Burnham, and Streifer.[1] The basic geometry of that device is shown in Fig. 1a. The reported device, consisting of 10 diodes with an electrode width of 3 μm and a center-to-center spacing of 10 μm, operated coherently (phase locked) up to a total optical output power of 150 mW. More recently, Scifres et al. reported a 40-element device, bonded to a copper heatsink, that exhibited coherent optical outputs up to 640 mW.[2] The purpose of this report is to explain the limitation on coherent output seen for these devices in terms of the temperature variations between array elements. Changes in heatsink design that will permit coherent operation of phase-locked GaAs arrays up to their maximum output power levels are also suggested.

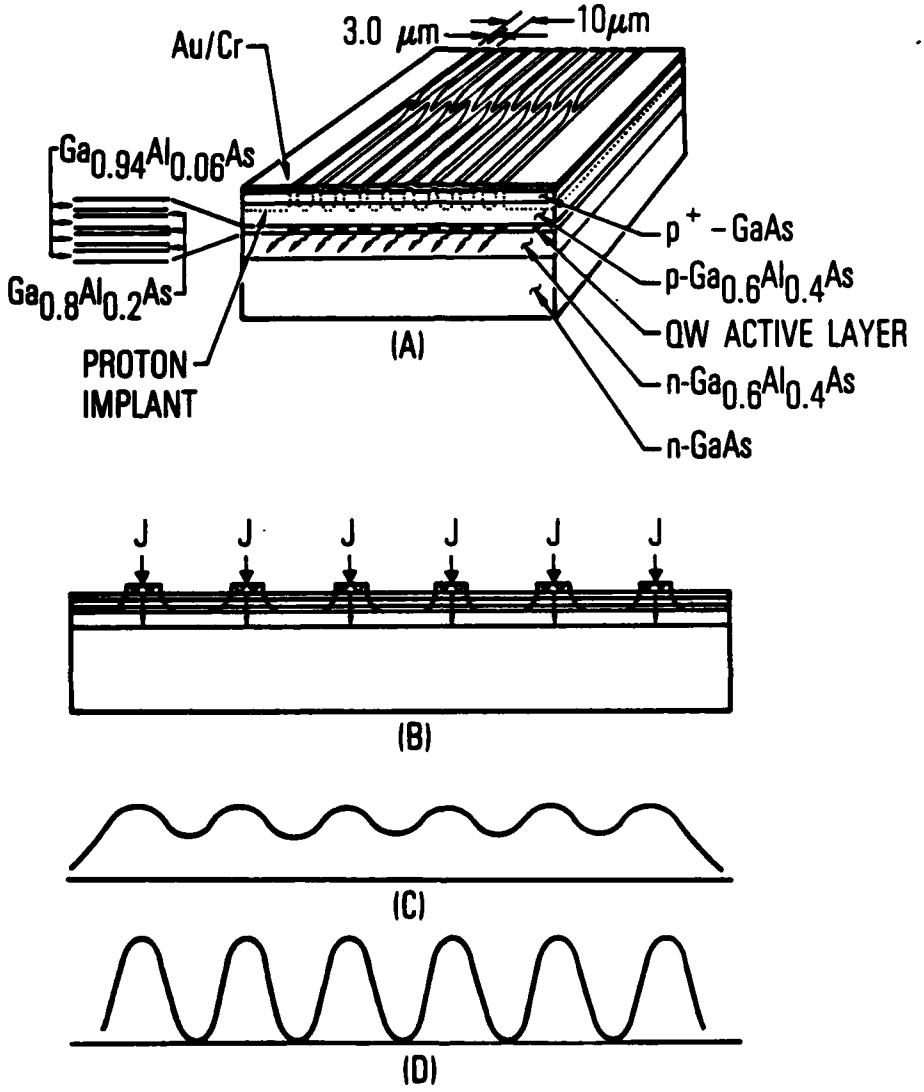


Fig. 1. Quasibroad-Area Operation of the Laser Array Reported by Scifres et al. (Ref. 2). (a) Sketch of laser-array geometry. (b) Cross-sectional geometry of array, showing current J entering through electrodes and spreading out in the active region. (c) Gain as a function of position along the array. (d) Output light intensity as a function of position along the array.

II. ANALYTIC MODELING

Figure 1 helps to explain why a laser array may be modeled as a quasibroad-area laser. Although the electrodes inject current into narrow stripes (Fig. 1b), current spreading causes the current in the active region to be only partially modulated (Fig. 1c). Because of the nonlinearity of the gain, the near-field output profile shows considerably more spatial modulation than does the current in the active region (Fig. 1d). For these reasons, the thermal properties of these laser arrays are very close to those of a broad-area laser and may be modeled by solving Poisson's equation for heat flow in that limit. This can be seen by referring to Fig. 2. The following assumptions will be made:

1. The heat flow in the substrate will be roughly the same as if the heat source were continuous.

2. The heatsink has a much lower thermal impedance than the GaAs substrate, so that all the heat is removed through the heatsink.

3. The heat flow in the epitaxial layers is uniform and linear.

4. The heat flow in the heatsink obeys LaPlace's equation for a uniform rectangular heat source placed on a semi-infinite heatsink (Fig. 2b). This approximation is altered when the diode array is placed at the edge of the heatsink to facilitate output coupling.

5. It is assumed and it will be shown below that of all the epitaxial contacting and bonding layers, only the GaAlAs (gallium aluminum arsenide) layer contributes significant thermal impedance.

With these assumptions, the model used to calculate the temperature rise in a diode array is that shown in Fig. 2b, in which a uniform rectangular heat source at temperature $T_2(y)$ is placed above a GaAlAs epitaxial layer of thickness d. This, in turn, provides a heat source at temperature $T_1(y)$ to the top of a semi-infinite heatsink; the heat source is held at value T_0 far from the heat source. The assumption is made that a power P flows downward through the device and that no heat is dissipated upward.

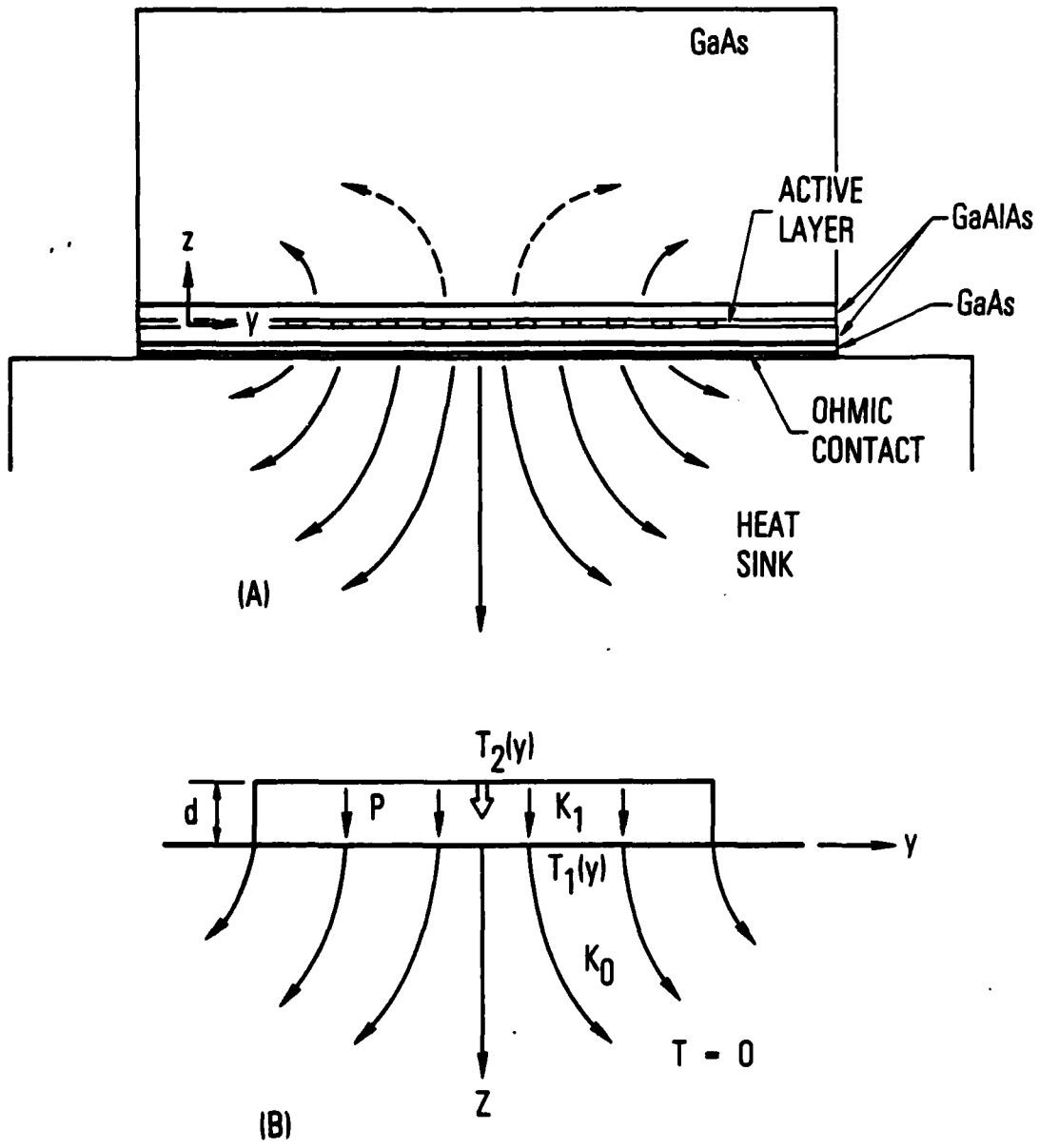


Fig. 2. Models of Heat Flow in a Quasibroad-Area Laser. (a) Heat flow from an array of heat sources in the active region surrounded by GaAlAs epitaxial layers. The GaAs substrate above the active layer provides only a small amount of heat dissipation into the air. (b) Heat flow used in this report, assuming a broad-area heat source, linear dissipation in the epitaxial layers, and power P dissipated into the heatsink. The thermal conductivities are K_1 and K_0 and the layer thickness is d.

In practice, the heatsink will not be semi-infinite, but must be shaped so that light may exit the diode, as shown in Figs. 3a and 3b. In addition, if diamond is used as a heatsink, it is noted that typical diamond heatsinks, which are commercially available, come in sizes no larger than a 1-mm cube and are typically placed on copper blocks for additional heatsinking. Then the exact thermal analysis must be done by computer. However, one other simple model for which an approximate solution may be obtained is that shown in Fig. 3b, in which the diode is placed at one edge of a heatsink that is assumed to fill a quadrant in space. Symmetry arguments say that this single-sided heat flow problem is just half that of the symmetric heat flow for a diode array twice as long, as shown in Fig. 3c.

Considering linear heat flow through the epitaxial layers, the temperature drop from the active region to the surface of the heatsink is given by

$$T_2(y) - T_1(y) = \frac{P}{A} \sum_i \left(\frac{d_i}{K_i}\right) \tag{1}$$

where P is the total power dissipated, A is the area of the quasibroad-area electrode structure, and d_i and K_i are the thickness and thermal conductivity, respectively, of each epitaxial layer or bonding layer. In Table 1 the thermal conductivity, typical layer thicknesses, and values of d/K for each of the layers that may be used in these devices are listed. It can be seen that only the GaAlAs layer has significant thermal impedance, and therefore only this layer will be considered in this analysis. The temperature drop in the epitaxial layers is thus assumed to be

$$t_2 = T_2 - T_1 = \frac{Pd_1}{AK_1} \tag{2}$$

The temperature drop from the surface of the heatsink to far inside the heatsink is calculated from LaPlace's equation for heat flow from a rectangular source into a semi-infinite volume. The temperature on the heatsink surface (z = 0) for an array of width 2W and length L (Fig. 3b) or width 2W and length 2L (Fig. 3c) can be written[3,4] as

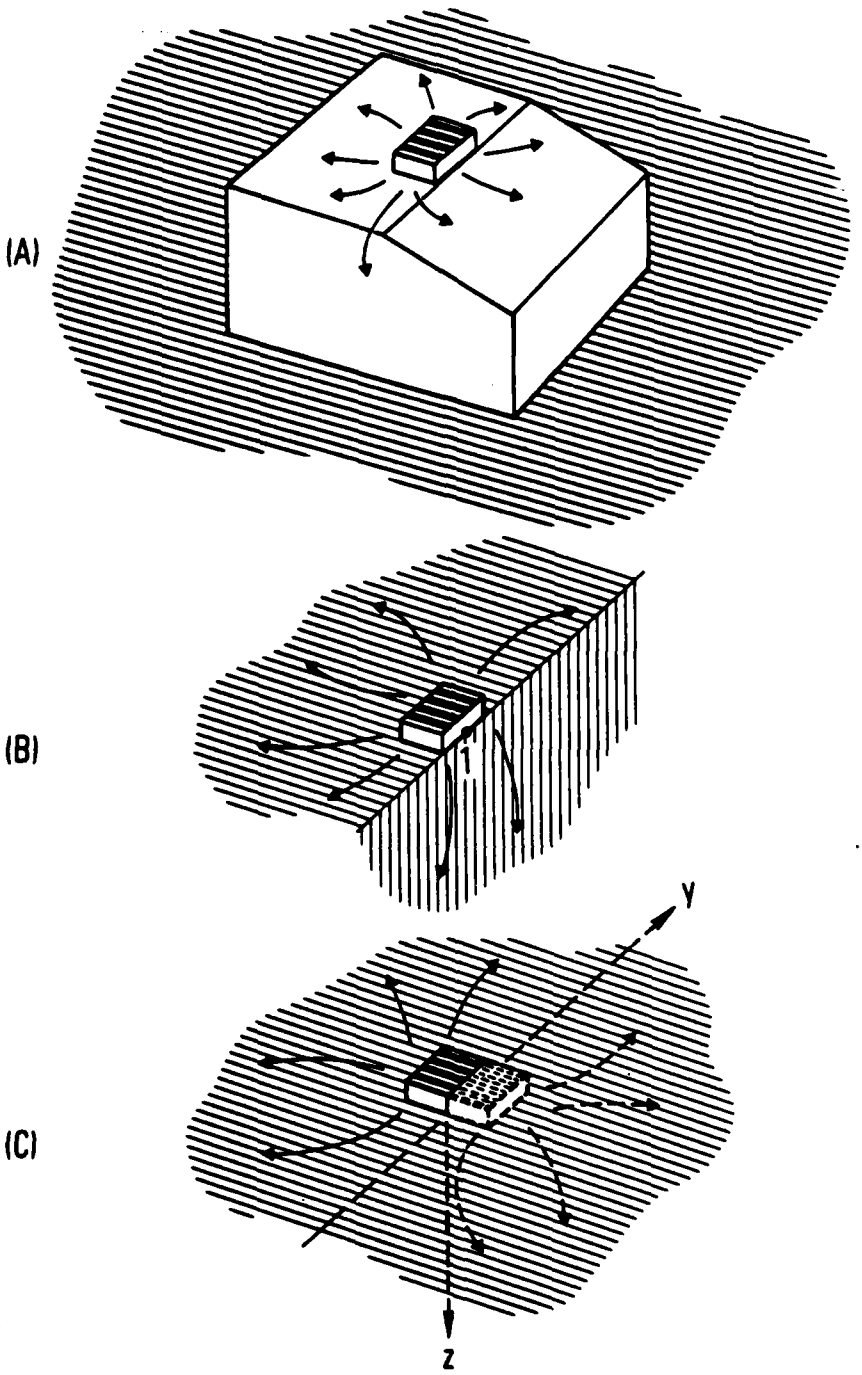


Fig. 3. Three Geometries for Heatsinks. (a) Heatsink cut to allow light to leave the laser array. (b) Diode array placed at the edge of a heatsink that fills a quadrant of space. (c) Diode array of twice the above length, placed on a semi-infinite heatsink. By symmetry, the solution to this problem is the same as that shown in (b), above.

Table 1. Thermal Conductivities, Typical Layer Thicknesses, and Thermal Impedances for Typical Materials Used in Double Heterostructure Lasers

Material	Thermal conductivity K_i, W/cm.K	Typical thickness d_i, μm	Thermal impedance d_i/K_i, $cm^2.K/W$
$Ga_{0.7}Al_{0.3}As$	0.14	2	14×10^{-4}
GaAs	0.45	0.5	1.1×10^{-4}
Indium	0.87	0.2	0.23×10^{-4}
SiO_2	0.01	0.2	20×10^{-4}
Copper	4	∞	
Diamond	20	∞	

For alternating stripes of SiO_2 and indium:

$$\left(\frac{d}{K}\right)_{eff} = \frac{10}{\frac{3K_1}{d_1} + \frac{7K_2}{d_2}} \qquad 0.75 \times 10^{-4}$$

$$T(x, y, 0) = T_0 + \frac{q}{2\pi K} [G(W + y, L + x) + G(W + y, L + x)$$

$$+ G(W + y, L - x) + G(W - y, L - x)] \quad (3)$$

where $$G(x, y) = x \sinh^{-1} \frac{y}{|x|} + y \sinh^{-1} \frac{x}{|y|}$$

In this case, T_0 is the temperature at infinity and q is the uniform heat flux into the array area. The maximum temperature rise above ambient is

$$t_1 = T(0, 0, 0) - T_0 = \frac{P}{\pi KLW} \left[L \sinh^{-1} \left(\frac{W}{L}\right) + W \sinh^{-1} \left(\frac{L}{W}\right)\right] \quad (4)$$

where P is the power (in watts) from an array of width 2W and length L. For a device geometry similar to that reported by Scifres et al.,[1] the temperature rise in the epitaxial layers t_2 is calculated to be 5.6°C/W of dissipated power, while t_1 for a copper heatsink is 10.5°C/W; the result is a predicted total temperature rise of 16.1°C/W. This corresponds well to the measured thermal resistance of 12 - 20°C/W of applied power quoted in Ref. 1 and indicates that this thermal analysis is reasonably accurate.

At the center of the array length (shown by the y axis in Fig. 3c), the thermal distribution from Eq. (3) is given as

$$T_c(y) = T_0 + T(0, y, 0) \quad (5)$$

In the left-hand portion of Fig. 4, $T_c(y) - T_0$ is plotted as dots for two different-sized arrays. The array temperature averaged over its length is given analytically by

$$T_{av}(y) = \frac{1}{L} \int_0^L T(x, y, 0)dx$$

$$= T_0 + \frac{q}{2\pi KL} [H(2L, W + y) + H(2L, W - y)] \quad (6)$$

where

$$H(x, y) = xG(x, y) - \frac{y(x^2 + y^2)^{1/2}}{2} - \frac{x^2}{2} \sinh^{-1} \frac{y}{|x|} + \frac{y|y|}{2} \qquad (7)$$

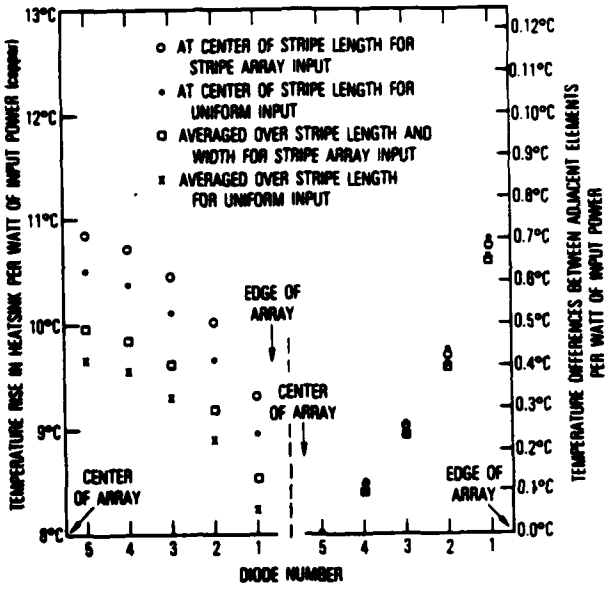
The temperature variation between diodes is obtained by calculating the temperature at values of y corresponding to the neighboring diode locations, then subtracting adjacent values. Since the temperature drop in the epilayers is nearly uniform, the temperature variation between diodes at the active region is approximately the same as that at the top of the heatsink. These temperature differences per watt of dissipated power for the laser diode array, mounted as shown in Fig. 3b, are given in Fig. 4, where $T_{av}(y_{n+1}) - T_{av}(y_n)$ is plotted as the value for the nth diode.

The quasibroad-area heat-source assumption breaks down when oxide-defined stripes are used. To analyze this case, assumption 1, above, is dropped. In the Appendix, expressions are given for the temperature on the top surface of the heatsink at the center of each heat source (stripe), as well as for the temperature averaged over diode length and width. That is, independent heat sources of the same overall array dimension are assumed to be applied to the heatsink surface. For comparison, these results are also plotted in Fig. 4.

To obtain the temperature in the active region, t_2 should be added to the values in Fig. 4. That is, a uniform 5.6°C/W should be added to those in Fig. 4 for the 10-element device, and 1.1°C/W should be added for the 40-element device.

It should be noted that the results given for a quasibroad-area heat source expressed by Eqs. (5) and (6) are within 10% of calculations determined by Eqs. (A-1) through (A-3). The somewhat higher temperature rise in the latter case occurs because of the concentration of the heat input into discrete regions.

(A)



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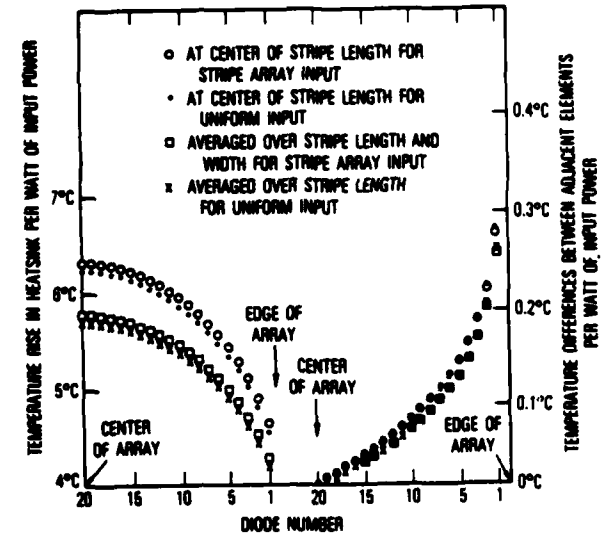

Fig. 4. **Thermal Profile for Two Diode Arrays, per Watt of Input Electrical Power. Diode no. 1 is at the edge of the array and the elements are numbered consecutively. Because of symmetry, only half the array is shown. The center-to-center spacing between diodes is 10 μm; the heat sink is copper. The points to the left show the temperature rise at the top of the heat sink at the position of each diode. The points to the right show the temperature difference between adjacent diodes. Figure 4a shows a 10-element array and Fig. 4b shows a 40-element array. The open circles are calculated from Eq. (A-1), the dots from Eq. (5), the boxes from Eq. (A-2), and the crosses from Eq. (6). The values for a diamond heatsink are one-fifth those for copper.**

III. SCALING TO LARGE ARRAYS

The output power reported from arrays of 10 stripes was limited by facet damage resulting from high local optical-field densities. For a given layer configuration, therefore, increased optical power may be obtained only by increasing the number of elements in the diode array. The output optical power will be a linear function of the number of elements in the diode array, as long as the heatsink can remove sufficient heat. However, the temperature rise is not a linear function of the array width; for the same input current density, the temperature rise at the center of the array increases less than linearly as the array is widened.

Figure 5 shows a plot of temperature rise [Eq. (5)] versus width for an array mounted on a copper heatsink. Also indicated is the potential output optical power available from such an array. A limit to operation of such wide arrays is the need to cool the copper heatsink to a temperature that will keep the operating temperature of the diode within a useful range (<85°C). Active cooling has been developed for other applications requiring large heat-flux removal and typically consists of flowing coolants in close contact with the heatsink. Through the use of cryogenic liquids it may be possible for the heatsink to be cooled to <100 K, which allows the total temperature rise to be as much as 200°C higher than that at the bottom of the heatsink. Referring to Fig. 5, this would predict that as much as 9 W can be produced from a 200-element laser array, if it operates at approximately 10% efficiency. Such a device may compete favorably with other laser sources for many applications. At these power and temperature levels, experimentally determined results[1,2] show conversion efficiencies from electrical to optical power of between 11% and 17%. At the assumed 10% efficiency, an electrical input of 90 W would be required to drive the diode array. The much higher thermal conductivity of diamond (Table 1) used as a heatsink may reduce the temperature rise considerably (see Section V).

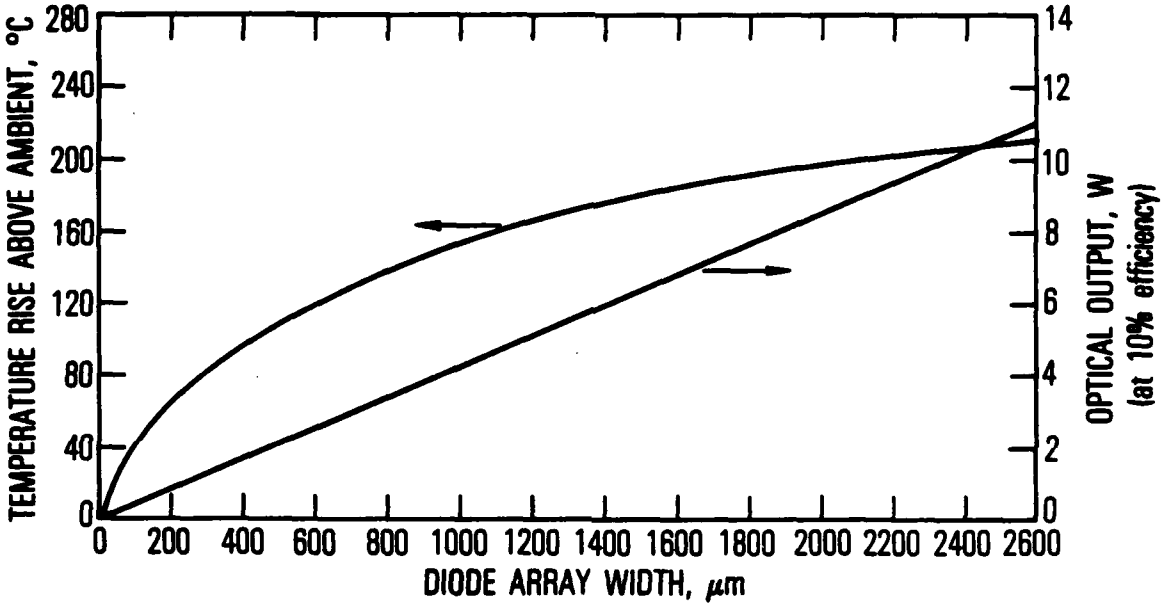

Fig. 5. Temperature Rise at the Center of the Surface of a Semi-infinite Heatsink, with Uniform Heat Applied over an Area of Length L and Width 2W for a Heat Flux of 1.6×10^4 W cm^{-2}. The optical output is for a diode operating at 10% efficiency.

IV. PHASE LOCKING

If the diode array is to operate phase locked, the temperature distribution across the face of the diode array becomes critical. In Section II, theoretical expressions for the temperature variation between diode elements were given. For the 10-element device reported by Scifres et al.,[1] which had an optical output of 0.4 W per facet for a total electrical power of 4.7 W (an efficiency of 17%), 3.9 W were dissipated as heat. From Fig. 4 it can be seen that the temperature variation between diodes ranged from 0.4°C to 2.6°C. The total temperature variation is 6.0°C. Given the well-known fact that the laser wavelength changes with temperature by roughly 3 Å per degree centigrade, adjacent stripes will tend to have a wavelength difference of from 1.3 Å to 7.8 Å and a total wavelength range of 17.9 Å. With such wavelength variations, phase locking will be difficult without large amounts of optical coupling.

When two coupled parallel lasers differ in resonance wavelength by $\delta\lambda$, the lasers can be locked as long as[5]

$$\delta\lambda < \frac{\lambda^2}{2\pi nL}\,\Gamma \tag{8}$$

where Γ is the fraction of optical power coupled from one laser into the adjacent laser. We use this expression in the absence of an analysis for the coupling conditions for multiple parallel lasers. Assuming that the coupling were 100%, then the maximum wavelength separation between lasers that can lock is given by $\Gamma = 1$, or $\delta\lambda = 1.3$ Å when $\lambda = 0.83$ μm, $L = 250$ μm, and $n = 3.5$. At 3 Å/°C this wavelength requirement corresponds to a maximum temperature variation between lasers of 0.4°C. Referring to Fig. 4, the temperature variation between all but the outside stripes is less than this maximum at 0.96 W of electrical power input. At a reported output efficiency of 17%, this corresponds to optical powers of 160 mW.

The thermal analysis seems to indicate that locking of the inner stripes cannot occur at optical powers greater than about 160 mW. This agrees with

the Scifres et al. report that phase locking was not seen above an output power of about 150 mW. The thermal analysis also indicates that the outer stripes are considerably cooler than the inner ones and will undoubtedly be the first ones to lose phase locking. The reader is reminded that the two-stripe analysis is only an approximation of the multiple-stripe analysis and that the impact of the overall 3°C temperature variation between the center and outer stripes must be theoretically explored before an accurate comparison with experiment can be made.

The phase-locking criteria for a 40-element array can be determined from Fig. 4b. Consider the reported array,[2] which emits up to 1.5 W per facet with an output power conversion efficiency of 13%. When the input power dissipated is 20 W and the heatsink is copper, Fig. 4b shows that the temperature drop between adjacent diodes averages about 1.6°C. These diodes cannot be phase locked at this power level, however, because this would cause an average 5-Å wavelength difference between diodes. Scifres et al.[2] indicated that phase locking occurred up to output optical power levels of 0.32 W per facet, which occurs with an input-dissipated power of about 4.3 W. This causes an estimated temperature drop per diode of 0.36°C, which corresponds to a wavelength difference between adjacent diodes of 1.1 Å. According to Eq. (8), these lasers can be phase locked since $\Delta\lambda < 1.3$ Å. Thus, the model invoked here accurately describes the experimental results.

A given diode array on a copper heatsink will lose phase locking if driven too hard. However, we will show that if a diamond heatsink is used, phase locking of adjacent elements remains even up to power levels that cause catastrophic damage. In the next section we first examine, in a general way, the use of diamond as a heatsink; then we examine the use of a shaped heatsink to limit temperature variation between diode elements.

V. THE USE OF A DIAMOND HEATSINK

It is of general interest to consider the possibility of using a type-II diamond heatsink rather than a copper one, since diamond's thermal conductivity is five times higher than that of copper. In this case, the temperature at the surface of the heatsink will be less than if copper is used, because diamond can more effectively carry away the heat than can copper. The temperature rise will therefore be decreased by a factor of five, the ratio of the thermal conductivities. Thus, for a diamond heatsink and the 10-element array, t_1 = 2.1°C/W, rather than the 10.5°C/W for copper which was calculated in Section II. Adding this temperature rise to the temperature drop within the epitaxial layers, the temperature of the active region will be $t_1 + t_2$ above the heatsink temperature, i.e., 7.7°C/W. When compared to the temperature rise for a copper heatsink, this predicts a decrease by a factor of two in the temperature rise of the active region caused by the heatsink temperature. This decreased heating of the active region should lead to increased performance of the array.

It is important to point out that the expected improvement in array performance for diamond heatsinks is unique to the array geometry and is not a characteristic of single-stripe diodes. Joyce and Dixon[3] showed that for a single-stripe laser, there is no real advantage in using a diamond heatsink rather than a copper one, because of the large amount of heat loss in the GaAlAs. However, the array has a very different geometry and the heatsink plays a much larger role. The power output of the array relies ultimately on the ability of the heatsink to remove the heat as rapidly as possible.

The ability of the diamond heatsink to remove more heat than can a copper heatsink makes it possible to scale the published 10-element array to many times that width, consistent with removal of the heat by the heatsink. The properties of the heatsink provide the ultimate limitation to the maximum amount of power that can be achieved reliably from a diode array.

The output power reported from 10-diode arrays was limited by facet damage resulting from high local optical-field densities. For a given

epilayer configuration, therefore, increased optical power may be obtained only by increasing the number of elements in the diode array. The output optical power will be a linear function of the number of elements in the diode array, as stated in Section III, as long as the heatsink can remove sufficient heat. Because of its higher conductivity, a diamond heatsink makes possible larger arrays than does a copper heatsink, since it can more effectively remove heat.

The width of a diamond-heatsinked array that produces the same temperature at its center as a smaller copper-heatsinked array may be determined from Fig. 5 by considering the relative conductivities. Indeed, it is easily seen that a 2500-μm array mounted on diamond produces at its center the same temperature as the 100-μm array mounted on copper, given the same input current density. This limit cannot be reached at this time, however, since commercially available diamond heatsinks are limited to approximately 1 mm in width.

In addition to making larger arrays possible, the higher conductivity of diamond makes possible much more uniform temperature operation and better phase locking. This is shown by scaling the results of Section IV to the case of a diamond heatsink. That means that the free-running wavelength difference between adjacent laser elements in a 10-element array will range from 0.3 Å to 1.5 Å, with a total spectral range of 3.6 Å at the output optical power level of 0.4 W.

A diamond heatsink will allow five times the power to be dissipated, with the same temperature rise between stripes, since Eq. (3) is inversely proportional to the thermal conductivity of the heatsink. Thus, assuming the efficiency remains the same, the diamond heatsink will allow five times the optical power, or up to 750 mW from a 10-element array, before phase locking is destroyed. With the 40-element array, the diode array would maintain phase locking to five times the optical power level of 0.32 W per facet, or 1.6 W per facet. Catastrophic damage was measured at 1.5 W per facet; thus, this

array, if placed on a diamond heatsink, may remain phase-locked at all achievable power levels if the approximate analysis of this report is valid under these conditions.

VI. THE USE OF A SHAPED HEATSINK

We have also considered the possibility of shaping the heatsink to obtain better temperature uniformity. We will show that much greater temperature uniformity is obtained by considering heatsinks that are not infinite quadrants but have a cross-sectional shape that acts to improve the temperature uniformity. This study required an analysis that was most conveniently handled by the PATRAN and NASTRAN computer programs.

Four heatsink designs have been thermally analyzed. The first two of these are shown in Figs. 6a and 6b. Here, the dimensions of the laser array are matched to the tip of the heatsink. Two array sizes were chosen for analysis, 250 × 250 μm and 1000 × 250 μm, representing 25- and 100-element arrays, respectively. The latter size was chosen because it was the largest array that could be mounted on a commercially available type-II diamond heatsink.

The heatsink was designed in two parts: (1) a cap region consisting of copper or diamond, and (2) a base region consisting of copper. Figure 6 shows the cap for each device. The cap for the smaller array was a truncated pyramid 1 mm high, 1 mm square at the base, and 250 μm square at the top (Fig. 6a). For the larger array, the cap region was designed as a wedge 1 mm high, 1 mm square at the base, and 1 mm by 0.25 mm at the top (Fig. 6b). The base region was designed similarly to Fig. 6a, as a truncated rectangular pyramid, but 5 mm high, 5 mm square at the base, and 1 mm square at the top.

As an aside, note that the exterior angle between the array and heatsink is 140°, which means that the heatsink will not interfere with light diffracting from the laser. While this heatsink geometry is not optimum, it has symmetry to simplify the computer analysis and serves to demonstrate the concept that a more uniform temperature operation can be achieved by using shaped heatsinks.

The thermal analysis was performed with PATRAN, an interactive finite-element array-generation program, and NASTRAN, a structures and thermal

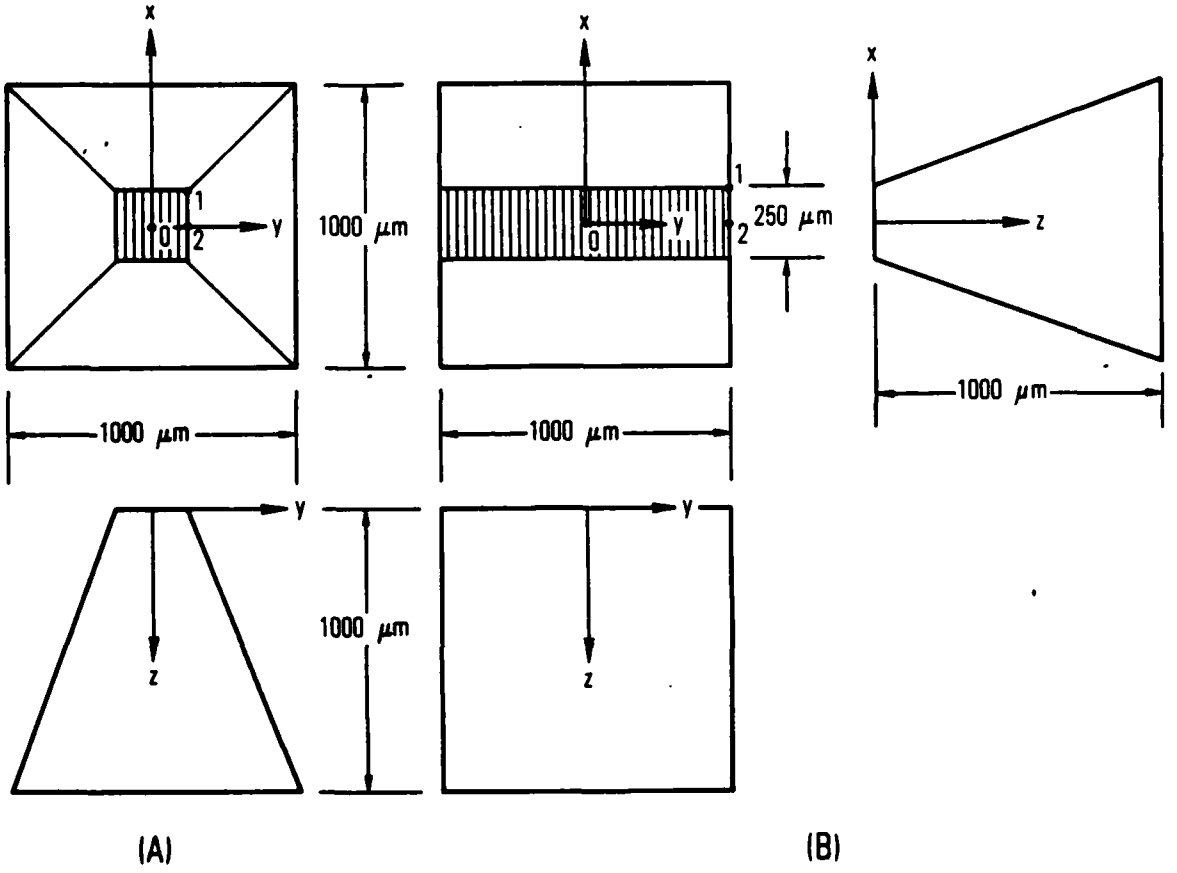

Fig. 6. Cap Region for a Heatsink Designed to Decrease the Temperature Variation across a GaAs Laser Array (shown striped in the drawing). (a) Pyramidal design for a 25-element 250 × 250-μm array. (b) Wedge design for a 100-element 250 × 1000-μm array.

finite-element analysis program. Because of symmetry, only one fourth of the design is actually modeled by PATRAN and NASTRAN. Adiabatic conditions are assumed where air contacts the walls; so that radiative and conductive losses to air can be ignored. Both base and cap were divided into 343 hexagonal regions, with 512 nodes defined for each region. The temperature at the base of the large copper heatsink was prescribed as 290 K, while the surface in contact with the diode had a uniform heat input of 1.6×10^4 W cm^{-2}, or 10 W for the 250 × 250-μm array and 40 W for the 250 × 1000-μm array. Thermal conductivities of 20 W/cm K and 4 W/cm K were used for diamond and copper, respectively.

Table 2 lists the average temperature rise ΔT_0 of the heatsink surface above ambient, the maximum temperature variation in the y direction ΔT_{02}, and the maximum temperature variation from the center of the array to the outside corner ΔT_{01}, for the two array sizes (designs no. 1 and no. 2) and cap materials. (See Fig. 6 for the location of points 0, 1, and 2.) These results show dramatically the effect of the heatsink on the temperature variation along the array (y direction). Compare the value for T_{02} in designs no. 1 and no. 2. The low temperature variation in design no. 2 is caused by the vertical walls at the end of the heatsink.

A consideration of the heat-flow lines in the y-z plane (Fig. 6) will show they are only parallel to the z axis for small z, which causes negligible variation in temperature along the y axis. Heat flow still occurs in the x direction, as shown by the much larger value of T_{01}. The price to be paid for this shaped heatsink is, of course, a somewhat increased operating temperature. The values in Table 2 are for an electrical input of 10 and 40 W, respectively, so that the temperature rise per watt is 13 and 6°C, respectively, comparable to that calculated for the semi-infinite copper heatsink (Fig. 4).

These results show that the heatsink must be truncated at the edge of the array if more temperature uniformity for phase locking is to be obtained, and that the penalty in increased operating temperature may be only moderate.

Table 2. Temperature Variations over Various Arrays

Design no.	Array width, μm	Cap width, μm	Diamond cap (K = 20 W/cm °C)			Copper cap (K = 4 W/cm °C)			Input power, W
	W		ΔT_0	ΔT_{02}	ΔT_{01}	ΔT_0	ΔT_{02}	ΔT_{01}	P
1	250	250	47	1.3	3.1	130	6.4	12	10
2	1000	1000	90	0.01	1.5	242	0.02	7.3	40
3	100	100	24	0.1	0.1	77	0.55	0.84	4
4	100	∞	7.3	1.2	2.1	36	6.2	10.4	4
5	400	1000	35	6.5	11	76	9.5	39	16
6	400	400	41	0.1	8.5	113	0.11	39	16
7	400	∞	17	5.4	5.8	84	27	34	16

Design no. 1: Double truncated pyramid (Fig. 6a).
Design no. 2: Pyramid base and wedge cap region (Fig. 6b for cap).
Design no. 3: Truncated pyramid base, pyramid cap with constant cross-section plateau (Fig. 7).
Design no. 5,6: See Fig. 3a.
Design no. 4,7: Semi-infinite heatsink.

All devices have a thermal load of 1.6×10^4 W/cm^2.

On the basis of results for the 25- and 100-element array designs, a heatsink was designed for the 10-element array discussed in Sections I through IV. The copper base assumed for designs no. 1 and no. 2 was retained, while the cap was redesigned to lower its thermal resistance and reduce temperature variations between array elements. Figure 7 shows the cap for this design. Results of calculations based on this design are given as no. 3 in Table 2. For comparison, the calculated temperature rise and temperature variation for the semi-infinite heatsink are shown as design no. 4. The temperature variation is reduced by more than an order of magnitude, while the overall temperature increases by only a factor of two or three. This design is an example of the trade-off that must be made between temperature variation and thermal loading.

Finally, since the above designs may be difficult to fabricate and the objective was to obtain a minimum temperature variation between diode elements and not necessarily along diode length, another fairly simple heatsink design was also considered. It consisted of a copper base 2 cm long by 1 cm wide and 1 cm high, with half the top surface cut off at a 30° angle to the base (Fig. 3a). The slanted section minimizes optical diffraction effects. A diamond pad 250 μm thick was mounted on the centerline of the copper base so that the edges of the pad and the base coincided. Two pad dimensions were analyzed: 1 mm by 1 mm (design no. 5) and 400 μm by 1 mm (design no. 6). Uniform heat was applied to the top surface of these pads over dimensions comparable to those of a 40-element array, namely 400 by 250 μm. The array was assumed to be bonded at the leading edge of the diamond, along the centerline of the pad. Results of the thermal analyses for these designs and for the semi-infinite heatsink with no diamond pad (design no. 7) are also included in Table 2.

These designs again show dramatically how important it is for the lateral dimension of the heatsink to match the dimension of the array. The smaller heatsink reduced the temperature variation by an order of magnitude or more. In addition, the temperature rise per watt for the smaller heatsink is considerably less than that in the previously optimized design no. 3; in fact,

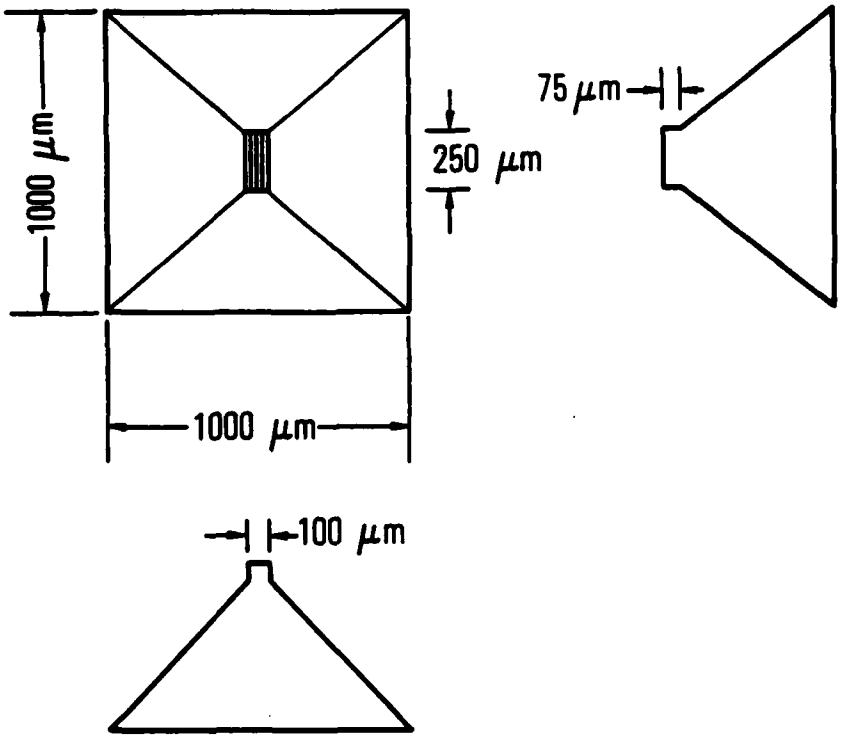

Fig. 7. **Cap Region for a Heatsink Designed to Provide a Minimum Temperature Variation across a 10-element GaAs Laser Array (shown striped in the drawing).**

the temperature rise is only a factor of two less than that for the semi-infinite heatsink, design no. 7. Design no. 6, which uses a diamond cap, should clearly be able to phase lock with only a 41°C temperature rise in the heatsink, for a 16-W electrical input (1.6-W optical power output, at 10% efficiency).

VII. CONCLUSIONS

The analysis of specific computer calculations shows that a minimum temperature variation across a diode array occurs when the heatsink is truncated abruptly at the edge of the array. This forces vertical heat flow near the surface over the entire array. Conversely, a semi-infinite heatsink creates the largest temperature variation because lateral heat flow cools the stripes at the array edge much more than it does those at the center. However, the overall temperature rise is much larger when lateral heat flow is excluded. Optimum heatsink design for a given application is, therefore, a trade-off between the need for lateral heat flow to decrease the overall temperature rise and the need for downward heat flow to achieve temperature uniformity.

We have shown that a substantial reduction in overall temperature rise and in temperature variation occurs if diamond, rather than copper, is used as a heatsink. The optimum design is a diamond pad, with the same width as the array, placed on a larger copper heatsink. The thickness of the pad will depend on the particular design requirements. For the cases considered here, a thickness of 100 to 250 μm for a diamond pad appears to be adequate to minimize the temperature variations sufficiently to ensure that the laser array operates coherenty to all power levels, up to those of catastrophic damage.

Analytic modeling of heat flow within a semi-infinite heatsink and the theory of phase locking (diffraction synchronization) of diode lasers[5] were used to explain the lack of coherent operation of 10- and 40-element laser diode arrays at higher output power levels.[1,2] In particular, the temperature variation between laser diodes is too great to allow locking, even at 100% coupling of elements. Finally, we have scaled the analysis to larger arrays and suggested the use of diamond heatsinks to ensure that phase locking occurs at all power levels.

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APPENDIX

For an array of N heat sources applied to the surface of the heatsink, the temperature anywhere on the heatsink surface is

$$T(x, y, 0) = T_0 + \frac{P}{4\pi NKLw} \sum_{i=-\frac{(N-1)}{2}}^{\frac{N-1}{2}} [G(y + w - ia, L + x) + G(w + ia - y, L + z) + G(y + w - ia, L - x) + G(w + ia - y, L - x] \quad \text{(A-1)}$$

where w is now one-half the stripe width, a is the diode spacing, and 2L is the diode length. The temperature averaged over the stripe length and width is given by

$$T_{AV}(y', 0) = \left(\frac{1}{2Lw}\right) \int_{-w}^{w} \int_{0}^{L} T(x, y, 0)dxdy$$

$$= T_0 + \frac{P}{8\pi NKL^2w^2} \sum_{i=-\frac{(N-1)}{2}}^{\frac{N-1}{2}} [F(2w + ia - y', 2L) + F(2w - ia + y', 2L) - 2F(ia - y', 2L)] \quad \text{(A-2)}$$

where

$$F(x, y) = \frac{xyG(x, y)}{2} - \frac{(x^2 + y^2)^{3/2}}{6} + \frac{(|x|^3 + |y|^3)}{6} \quad \text{(A-3)}$$

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